

5V to 3.3V

The circuit diagram shows a 5V to 3.3V voltage regulator. The input is a +5V source connected to the VIN pin (pin 3) of a 3-pin voltage regulator (u2). The regulator's GND pin (pin 1) is connected to a common ground. The output of the regulator (pin 2) is connected to a 22uF/16V capacitor (C1), which is then connected to a 22uF/16V capacitor (C2). The output of C2 is connected to a 0.1uF/16V capacitor (C4), which is then connected to a 0R/5% resistor (R1). The output of R1 is labeled P+3.3V and VCC3V3. A GND connection is shown at the bottom of the circuit.

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The diagram shows a download port (P4) with four pins. The connections are as follows:

- Pin 4: 2DAT signal line, connected to PA13 via a 10K resistor (R26).
- Pin 3: 2CLK signal line, connected to PA14 via a 10K resistor (R6).
- Pin 2: Connected to GND.
- Pin 1: Connected to GND.

The power supply is VCC3V3. The port is labeled P4 and SIP/2.54*4.

晶振

The diagram shows an 8MHz XTAL3225 crystal oscillator circuit. The crystal (X1) is connected between pins 1 and 2. Pin 1 is connected to HOSCI through capacitor C5 (20pF/50V) to GND. Pin 2 is connected to GND. Pin 3 is connected to GND. Pin 4 is connected to HOSCO through capacitor C6 (20pF/50V) to GND. The crystal is labeled 8MHZ/XTL3225.

主控芯片

TMF5003B LQFP64L

U1

1 VDD
2 PC13/DALI_TX
3 PC14/DALI_RX
4 PC15/HRPWM_FLT4
5 OSC_IN
6 OSC_OUT
7 MCLR
8 PC0/ADC0_IN6/ADC1_IN6
9 PC1/ADC0_IN7/ADC1_IN7
10 PC2/ADC0_IN8/ADC1_IN8
11 PC3/ADC0_IN9/ADC1_IN9
12 AGND
13 AVSS
14 VREF
15 PA0/DALI_TX/CMP3_OUT/ADC0_IN0
16 PA1/DALI_RX/I2C1_SMB/UART1_DE/ADC0_IN1
17 PA2/I2C1_SCL/UART1_TX/CMP0_OUT/ADC0_IN2/CMP0_INM_0
18 PA3/I2C1_SDA/UART1_RX/ADC0_IN3
19 AVSS
20 AVCC
21 PA4/DALI_TX/I2C1_SMB/UART0_TX/ADC1_IN0/DAC0_OUT/CMP0_1/2/3_INM_1
22 PA5/CAN_TX/DALI_RX/I2C1_SCL/UART0_RX/CMP3_OUT/ADC1_IN1/DAC1_OUT
23 PA6/CAN_RX/I2C1_SDA/UART0_DE/ADC1_IN2/DAC2_OUT
24 PA7/I2C1_SMBS/ADC1_IN3/CMP0_INP
25 PC4/UART0_TX/CMP3_OUT/ADC1_IN4/CMP3_INP
26 PC5/UART0_RX/ADC1_IN5/DAC3_OUT
27 PB0/ADC0_IN4/CMP1_INP
28 PB1/UART1_DE/HRPWM_EVT0/HRPWM_SCIN/HRPWM_SCOUT/CMP1_OUT/ADC0_IN5
29 PB2/CAN_TX/I2C0_SCL/UART1_TX/HRPWM_SCIN/ADC1_IN10/CMP1_INM_0
30 PB10/CAN_RX/I2C0_SDA/UART1_RX/UART1_TX/HRPWM_FLT2/ADC0_IN10
31 PB11/UART1_RX/HRPWM_FLT3/CMP2_INP
32 VSS
33 VCC
34 PB12/DALI_TX/HRPWM_OUT2A
35 PB13/DALI_RX/HRPWM_OUT2B
36 PB14/UART1_DE/HRPWM_OUT3A/CMP3_INM_0
37 PB15/HRPWM_OUT3B/CMP2_INM_0
38 PC6/HRPWM_EVT4/HRPWM_OUT5A
39 PC7/UART0_DE/HRPWM_FLT4/HRPWM_OUT5B
40 PC8/HRPWM_OUT4A
41 PC9/HRPWM_OUT4B
42 PA8/MCO/CAN_TX/UART0_RX/HRPWM_OUT0A
43 PA9/CAN_RX/UART0_TX/HRPWM_OUT0B
44 PA10/CAN_TX/I2C0_SMB/UART0_RX/HRPWM_OUT1A/CMP2_OUT
45 PA11/CAN_RX/I2C0_SMBS/UART0_TX/HRPWM_OUT1B/
46 PA12/CAN_TX/UART0_DE/HRPWM_FLT0/CMP0_OUT
47 PA13/SWDA/I2C1_SCL/HRPWM_FLT4/CMP2_OUT
48 VSS
49 VDD
50 PA14/SWCLK/I2C0_SDA/I2C1_SDA/UART1_TX/HRPWM_FLT5/HRPWM_SCIN
51 PA15/I2C0_SMB/UART0_SCL/UART1_TX/UART1_RX/HRPWM_FLT1
52 PC10/I2C0_SMBS/UART1_RX/UART0_TX/HRPWM_FLT4/HRPWM_FLT0
53 PC11/UART0_RX/HRPWM_EVT1
54 PC12/UART1_DE/UART0_DE/HRPWM_EVT0/HRPWM_FLT2
55 PD0/THRPWM_FLT5/HRPWM_FLT3/CMP2_OUT
56 PB3/SWO/I2C1_SCL/UART1_TX/HRPWM_SCOUT/HRPWM_EVT2/USB_DM
57 PB4/I2C1_SDA/UART1_RX/HRPWM_EVT1/USB_DP
58 PB5/I2C0_SMB/UART1_SCL/HRPWM_EVT5/CMP3_OUT
59 PB6/I2C0_SCL/I2C1_SMBS/UART0_TX/HRPWM_EVT0/HRPWM_SCIN/HRPWM_EVT3
60 PB7/I2C0_SDA/UART0_RX/HRPWM_EVT4/CMP1_OUT
61 BOOT
62 PB8/CAN_RX/I2C0_SCL/UART1_RX/HRPWM_EVT2
63 PB9/CAN_TX/I2C0_SDA/UART1_TX/HRPWM_EVT3/CMP0_OUT
64 VSS
65 VCC
66 GND

PC13
PC14
PC15
HOSCI
HOSCO
MCLR
PC0
PC1
PC2
PC3
AGND
VREF
PA0
PA1
PA2
PA3
AGND
AVCC
PA4
I2C1_SCL
I2C1_SDA
PA5
PA6
PA7
PC4
PC5
PB0
PB1
PB2
PB10
PB11
GND
VCC3V3
PB12
PB13
PB14
PB15
PC6
PC7
PC8
PC9
PA8
PA9
PA10
PA11
PA12
PA13
GND
VDD
PA14
PA15
PC10
PC11
PC12
PD0
PB3
PB4
PB5
PB6
PB7
PB8
PB9
GND
VCC3V3
GND

VDD
PC13
PC14
PC15
HOSCI
HOSCO
MCLR
PC0
PC1
PC2
PC3
AGND
VREF
PA0
PA1
PA2
PA3
AGND
AVCC
PA4
I2C1_SCL
I2C1_SDA
PA5
PA6
PA7
PC4
PC5
PB0
PB1
PB2
PB10
PB11
GND
VCC3V3
PB12
PB13
PB14
PB15
PC6
PC7
PC8
PC9
PA8
PA9
PA10
PA11
PA12
PA13
GND
VDD
PA14
PA15
PC10
PC11
PC12
PD0
PB3
PB4
PB5
PB6
PB7
PB8
PB9
GND
VCC3V3
GND

DIFF_OUT+
DIFF_OUT-
SELT_OUT
1WIRE_DQ
ADC2_IN1
ADC1_IN17
DAC_OUT
I2C1_SCL
I2C1_SDA
COMP_OUT
STA
UART1_TX
UART1_RX
GND
VCC3V3
CAN_TXD
CAN_RXD
UART0_RX
UART0_TX
TMS
JP2
SIP/2/2.54
TCK
JP1
SIP/2/2.54
1JTAG_TDO
SWO
USB_DP
KEY1
BOOT
BEEP
GND
VCC3V3
GND

TMF5003B_LQFP64L

芯片引脚引出端子

H1

Internal Pin	External Label
1	PC6
2	PC7
3	PC8
4	PC9
5	PC10
6	PA15
7	PC12
8	PC11
9	PB5
10	PD0
11	PB7
12	PB6
13	PC13
14	PB8
15	GND
16	VDD
17	PC15
18	PC14

H2

Internal Pin	External Label
1	VCC3V3
2	GND
3	PB15
4	PB14
5	PB13
6	PB12
7	PB10
8	PB11
9	PB1
10	PB2
11	PA1
12	PA4
13	AGND
14	AVCC
15	VREF
16	AGND
17	PA10
18	AGND
19	PA12
20	PA11
21	PA0
22	PA2
23	PC3
24	PC2
25	PC1
26	PC0
27	PB0
28	PC4
29	PC5
30	PC4

H3

Internal Pin	External Label
1	PA7
2	VCC3V3
3	PB9
4	+5V
5	PA3
6	BOOT
7	PA2
8	MCLR
9	PB3
10	
11	
12	
13	
14	
15	PA14
16	PA13
17	PB4
18	PB3
19	PA6
20	PA5
21	PA9
22	PA6
23	PA5
24	PA6
25	PA5
26	PA5
27	PA5
28	PA5
29	PA5
30	PA5

复位按键

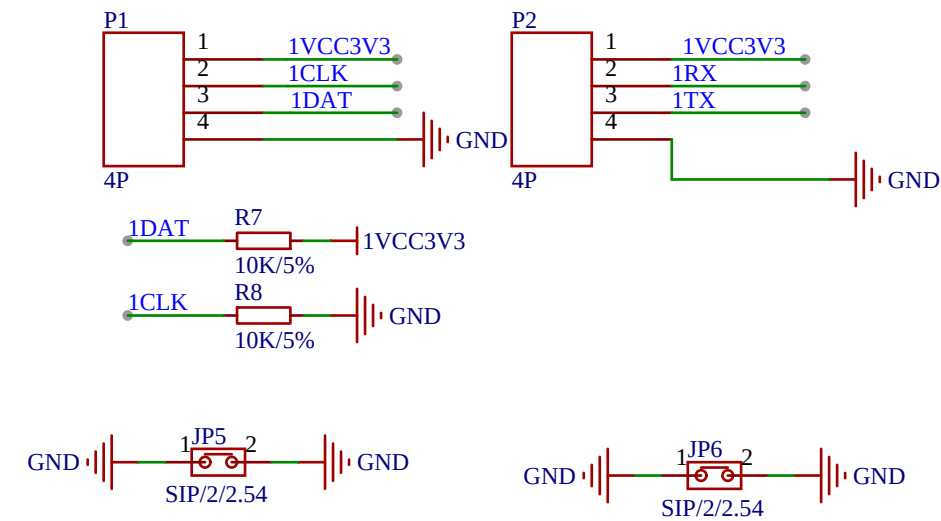
The diagram illustrates a reset key circuit. A green line labeled 'MCLR' is connected to a pull-up resistor 'R5' (10K/5%) which is connected to 'VCC3V3'. The other end of 'R5' is connected to a node that also branches to a capacitor 'C18' (0.1uF/16V) connected to 'GND', and to a push-button switch labeled 'RESET1 KEY'. The other side of the switch is connected to 'GND'.

模式选择

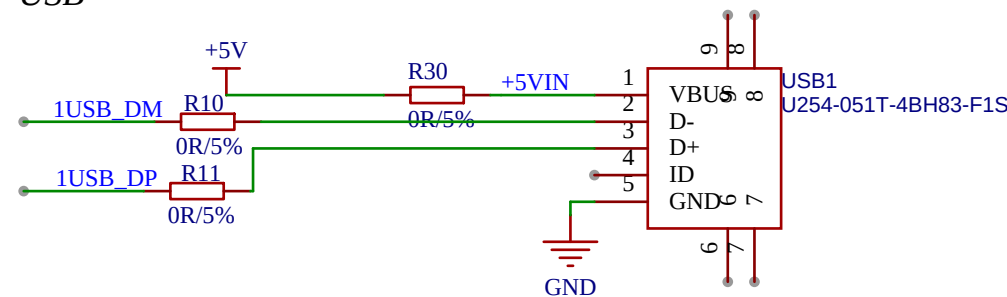
The diagram shows a 3-pin header P3 (SIP2.54_3P) with the following connections:

- Pin 1: Connected to VCC3V3 via resistor R19 (10K/5%).
- Pin 2: Connected to BOOT.
- Pin 3: Connected to GND via resistor R4 (10K/5%).

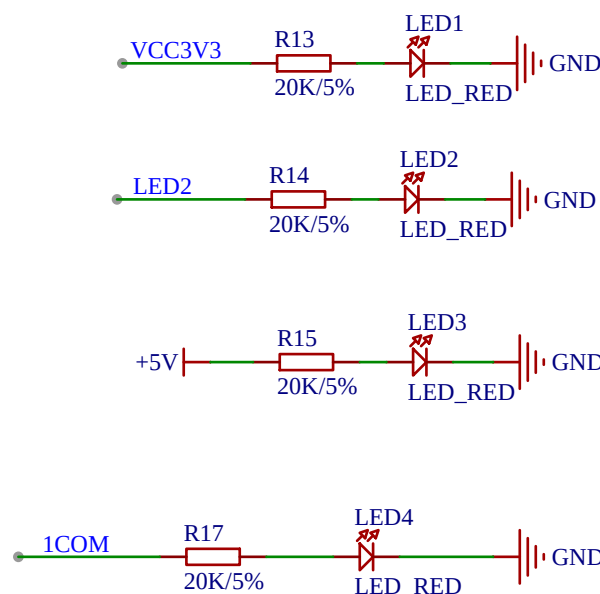
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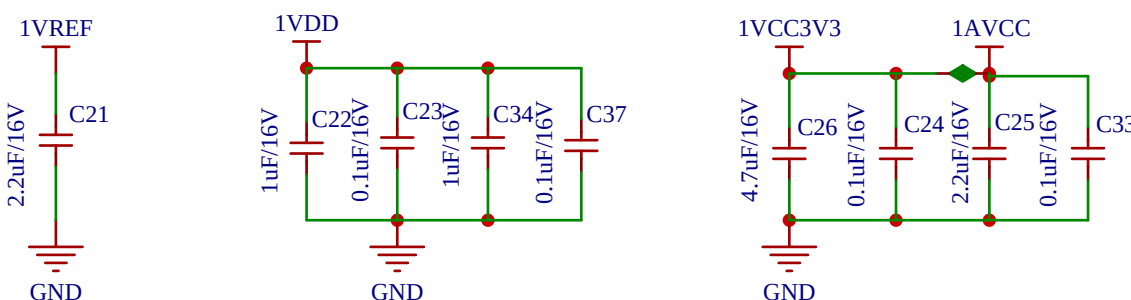
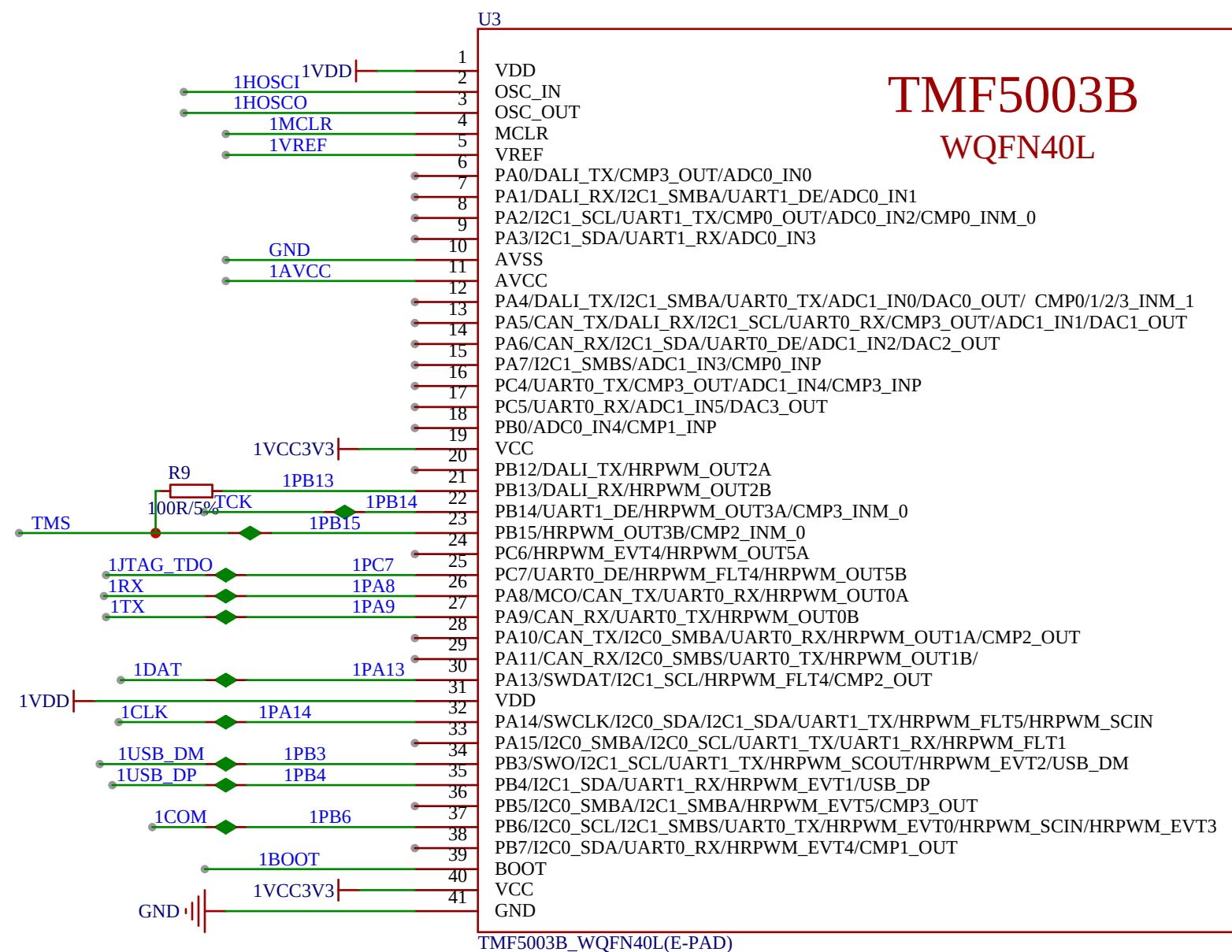
USB



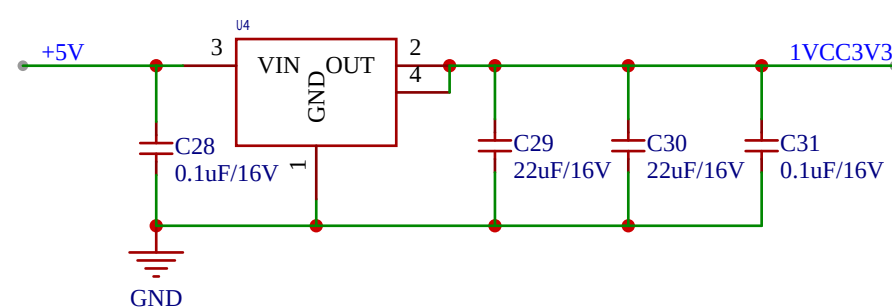
LED指示灯



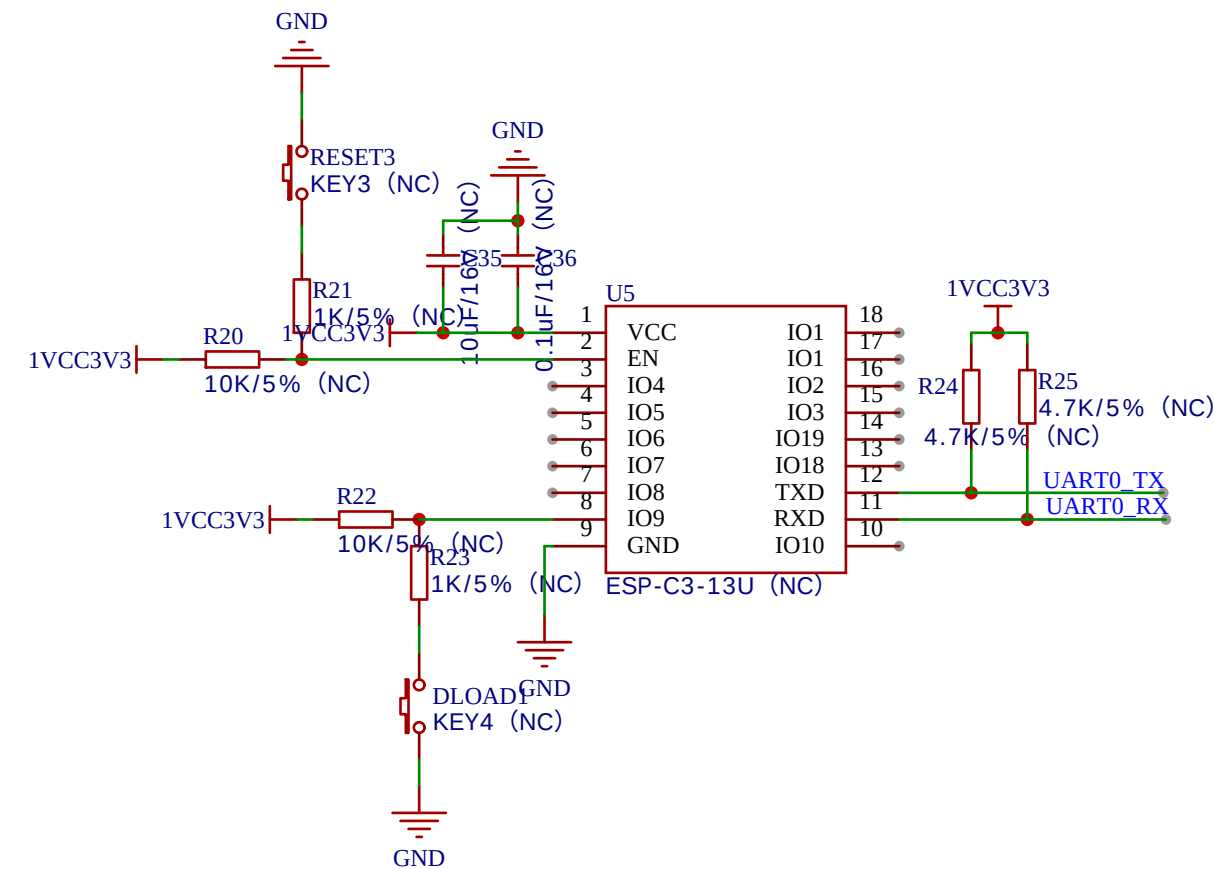
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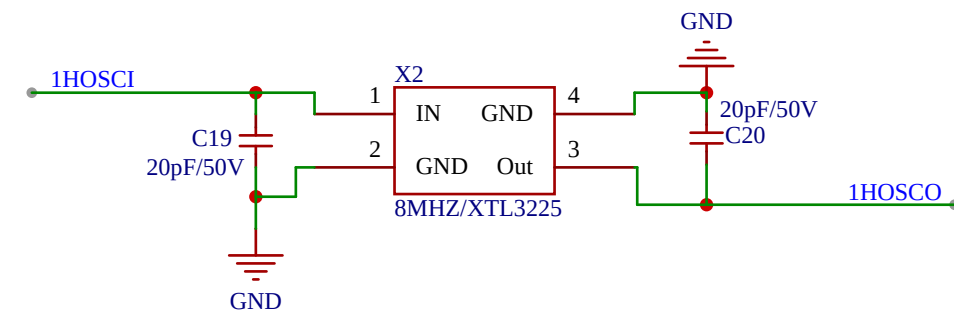
5V to 3.3V



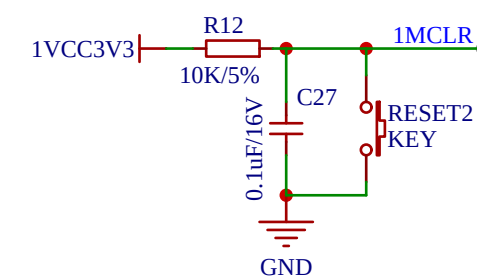
WIFI 模组



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复位按钮



模式选择



Project	TAE32F53XXTLF_EVAL_MINI_V1.02			
Drewed	WPP	 珠海泰为电子有限公司 Zhuhai Tai-Action Electronics CO., LTD.		
Reviewed	WLP			
VER	SIZE			
V1.0	A3	PAGE	2	OF 2